

CLAIMS

We claim:

1. A semiconductor device comprising:

a substrate;

at least one fuse formed within the substrate; and

an etch resistant layer over the at least one fuse.

2. The semiconductor device of claim 1, further comprising
an alignment mark formed on the substrate at a location
spatially removed from the fuse.

3. The semiconductor device of claim 2, wherein the
alignment mark further comprises the etch resistant layer
thereover.

4. The semiconductor device of claim 2, wherein the fuse and
the alignment mark are formed within a metal wiring layer of
the device.

5. The semiconductor device of claim 1, further comprising
at least one insulative layer above the etch resistant
layer.

1 6. The semiconductor device of claim 5, wherein the etch
2 resistant layer has a slower etch rate than that of the at
3 least one insulative layer thereabove.

1 7. The semiconductor device of claim 1, wherein the etch
2 resistant layer comprises silicon nitride.

1 8. The semiconductor device of claim 1, wherein the etch
resistant layer has a thickness of approximately 10-100 nm.

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1 9. A method of forming a fuse structure, comprising:
2 providing a substrate having at least one fuse formed
3 therein; and
4 depositing an etch resistant layer over a surface of
5 the substrate.

1 10. The method of claim 9, further comprising providing an
2 alignment mark formed within the substrate at a location
3 spatially removed from the fuse.

11. The method of claim 9, wherein the etch resistant layer
comprises silicon nitride.

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1 12. A method of performing a fuse deletion process,

2 comprising:

3 providing a substrate having at least one fuse therein,
4 an etch resistant layer over the fuse and at least one
5 insulative layer over the etch resistant layer;

6 removing a portion of the at least one insulative layer
7 above the fuse to the etch resistant layer; and

8 applying a radiant energy source to the fuse until the
etch resistant layer is partially removed.

13. The method of claim 12, further comprising providing an
alignment mark formed within the substrate having the etch
resistant layer and at least one insulative layer thereover.

14. The method of claim 13, wherein the fuse and the
alignment mark are formed within a metal wiring layer of the
substrate.

1 15. The method of claim 13, further comprising removing a
2 portion of the at least one insulative layer above an
3 electrical feature and the alignment mark while removing the
4 at least one portion of the at least one insulative layer
5 above the fuse.

1 16. The method of claim 12, wherein removing a portion of
2 the at least one insulative layer further comprises etching
the insulative layer.

17. The method of claim 12, wherein applying a radiant
energy source further comprises emitting a laser beam into
the fuse.

18. The method of claim 13, further comprising:

2 locating the alignment mark with the radiant energy
3 source; and

4 locating the fuse based upon the location of the
5 alignment mark.

